NEW SCHEME

CS46

USN | | | | | | | | | | |

Fourth Semester B.E. Degree Examination, July/August 2004

BM/EC/IT/TE/ML/EE/CS/IS

Computer Organisation

Time: 3 hrs.] [Max.Marks : 100

Note: *1. Answer FIVE Questions.*
2. All questions carry equal marks.

1. a) Consider the memory system of a computer storing the following data :

Address in Hex	Data stored (binary)
2000	00111000
2001	00110100
2002	00110010
2003	00111001

Interpret the storage as numbers in the manner indicated below and find their decimal values in each case.

i) Big-endian storage of 2 hex words of 4 - digits each

ii) Big-endian storage of 2 BCD words of 4 - digits each.

iii) Little - endian storage, in ASCII, of a 4 - digit signed hex word.

iv) Little endian storage, in ASCII, of a 4 - digit BCD word. (2 $\frac{1}{2}$ × 4 = 10 Marks)

(b) Give reasons to justify using, generally,

i) Single address instructions in 8 - bit CPU's

ii) Double address instruction in 16-bit CPU's

iii) Three address instructions in RISC systems

In each of these systems give assembly language programs for performing the operation :

data at mem A + data at meb B → memC. (10 Marks)

2. (a) What do you understand by stack frames ? Discuss their use in sub-routines. (10 Marks)

(b) Write an assembly program to multiply 2 memory arrays and store their result in a third memory array :

$a(i) * b(i) = c(i)$ for $i = 0$ to $n - 1$.
Consider load/store and 3-address system. (10 Marks)

3. (a) Explain how interrupt request from several I/O devices can be communicated to a processor through a single INTR line.

(b) Which type of I/o devices are interfaced through DMA ?
Explain the bus-arbitration process used for DMA. (10 Marks)

4. (a) Explain the general features of interfacing a parallel I/o port to a processor. **(10 Marks)**

(b)

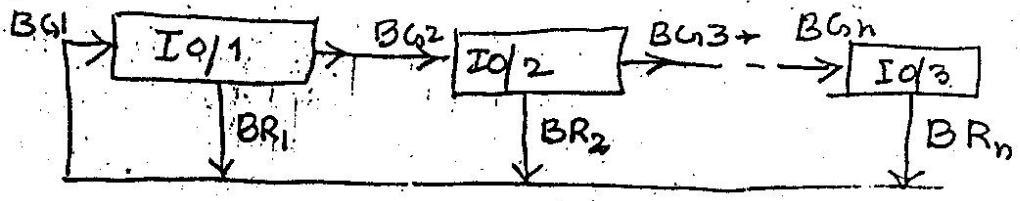

Fig Q 4b)

Consider the daisy chain arranement shown in fig Q.4b in which the bus request signal from the I/O is directly fed back as bus grant signal. Assume device IO/3 requests the bus and begins using it. When the device is finished, it deactivates BR3. Assume the delay from BG_i to BG_{i+1} in any device is d. Show that a spurious bus-grant pulse will travel down stream from device 3. Estimate the width of this pulse. **(10 Marks)**

5. (a) Describe SDRAM and DDR SD RAM operations for data transfer between main memory and cache memory systems. **(10 Marks)**

(b) Consider a processor running a program 30% of the instructions of which require a memory read or write operation if the cache bit ratio is 0.95 for instructions and 0.9 for data. When a cache bit occurs for instruction or for data, only one clock is needed while the cache miss penalty is 17 clocks to read/write on the main memory. Work out the time saved by using the cache, given the total number of instructions executed is 1 million. **(10 Marks)**

6. (a) Work out the multi level look - ahead carry scheme for doing a 32 bit number addition How many gate delays are required to do the complete addition in this method ? **(10 Marks)**

(b) The hexa decimal value of π is 3.243F6A8885A308D3... Work out the IEEE standard representation (IEEE standard 754-1985) of π in single and double precision formats. **(5+5 Marks)**

7. (a) Show the basic organisation of a CPU in terms of registers and other units for a single bus data path CPU. In such a CPU, show the complete action of the CPU in fetching and executing the instruction.

Load R_1 from memory data at A, where A is a memory address. Assume the instruction is in one process or word. Indicate the control signals to be used at each stage of execution. **(10 Marks)**

(b) Explain the basic concept of micro programmed control. **(10 Marks)**

8. (a) With a block diagram explain the general requirements of a microwave oven **OR** a digital camera. **(10 Marks)**

(b) Write short notes on any TWO.

i) A good method of hardware multiplication

ii) SCSI bus

iii) Virtual memory **(5+5 Marks)**

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